

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

Claims 1-124 (Cancelled)

2.1.26
¹²⁶
~~125~~ (New) A three-dimensional memory device with ECC circuitry comprising:
a support element;
error checking and correcting (ECC) circuitry carried by the support element; and
a memory array carried by the support element, wherein the memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another, wherein the memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers.

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¹
~~126~~ (New) The invention of Claim ¹²⁶~~125~~ further comprising a housing protecting the error checking and correcting (ECC) circuitry and the memory array.

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~~127~~ (New) The invention of Claim ¹²⁶~~125~~, wherein the memory cells comprise write-once memory cells.

⁹128¹²⁶ (New) The invention of Claim ~~125~~, wherein the memory cells are selected from the group consisting of semiconductor-transistor-technology-based memory cells, magnetic-based memory cells, and organic-electronics-based memory cells.

³⁰129 (New) A method for storing data and error checking and correcting (ECC) bits in a three-dimensional memory device with ECC circuitry, the method comprising:

(a) providing a three-dimensional memory device with ECC circuitry to a data storage system, the memory device comprising:

a support element;

error checking and correcting (ECC) circuitry carried by the support element; and

a memory array carried by the support element, wherein the memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another, wherein the memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers;

(b) with the memory device, receiving at least one data bit to be stored in the memory array;

(c) with the ECC circuitry, generating at least one ECC bit based on the at least one data bit; and

(d) storing the at least one data bit and the at least one ECC bit in the memory array.

¹
130. (New) The invention of Claim ¹³⁰~~129~~ further comprising:

(e) retrieving the at least one data bit and the at least one ECC bit in the memory array; and

(f) with the ECC circuitry, identifying an error in the retrieved at least one data bit and at least one ECC bit.

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131. (New) The invention of Claim ¹³⁰~~129~~, wherein the memory device further comprises a housing protecting the error checking and correcting (ECC) circuitry and the memory array.

³
132. (New) The invention of Claim ¹³⁰~~129~~, wherein the memory cells comprise write-once memory cells.

⁴
133. (New) The invention of Claim ¹³⁰~~129~~, wherein the memory cells are selected from the group consisting of semiconductor-transistor-technology-based memory cells, magnetic-based memory cells, and organic-electronics-based memory cells.

⁵
134. (New) A system for storing an error checking and correcting (ECC) bit in a three-dimensional memory array, the system comprising:

a data storage system; and

a memory device adapted to be releasably coupled to the data storage system, the memory device comprising a memory array carried by the support element, wherein the memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above

one another, wherein the memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers;

wherein the data storage system comprises error checking and correcting (ECC) functionality.

¹³⁵
138. (New) The invention of Claim ~~134~~, wherein the ECC functionality is implemented in software in the data storage system.

¹³⁵
138. (New) The invention of Claim ~~134~~, wherein the ECC functionality is implemented in a file system in the data storage system.

¹³⁵
137. (New) The invention of Claim ~~134~~, wherein the ECC functionality is implemented in hardware in the data storage system.

¹³⁵
138. (New) The invention of Claim ~~134~~, wherein the memory device further comprises a housing protecting the memory array.

¹³⁵
139. (New) The invention of Claim ~~134~~, wherein the memory cells comprise write-once memory cells.

¹³⁵
140. (New) The invention of Claim ~~134~~, wherein the memory cells are selected from the group consisting of semiconductor-transistor-technology-based memory cells, magnetic-based memory cells, and organic-electronics-based memory cells.